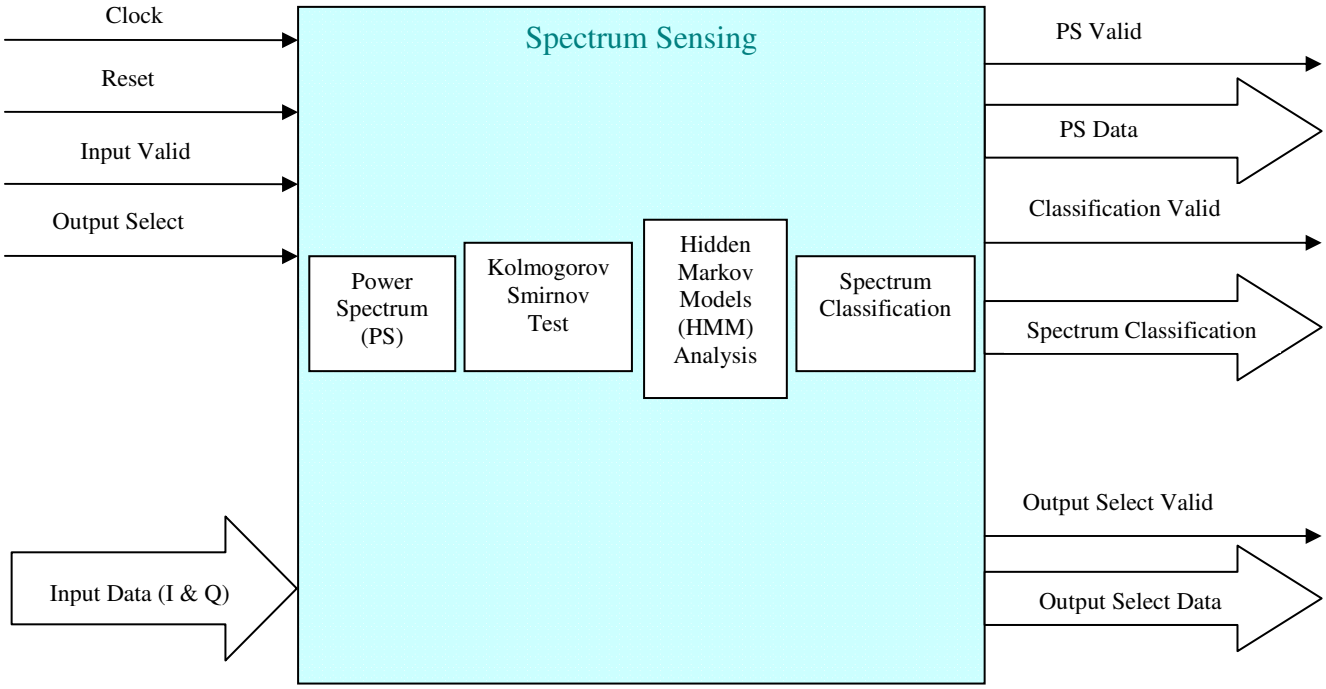
Spectrum Sensing Core



Features

- Parameterisable Input bit width
- Parameterisable FFT size
- Parameterisable HMM window length
- Parameterisable PS bit width
- Detects multiple interferers
- Fully synchronous design using only one clock
- Automatic internal rescaling
- Low latency
- Optimized design allowing high-speed operation
- User friendly control interface
- Silicon verified in multiple devices
- Can be tailored to customer needs
- Area/Power efficient architecture

Deliverables

- Netlist or synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- Integration documentation and user guide

Overview

The Spectrum sensing core blindly detects occupied sub-carriers within a wideband spectrum. The algorithm implemented in this core uses a patented algorithm (US 8,630,377 B2). The efficient real time implementation makes this core an ideal candidate to be used in cognitive radios. Spectrum sensing core is a fully parallel implementation which gives real time spectrum sensing capabilities allowing little to no interference to the incumbent. This spectrum sensing core is targeted to be used in radios developed based on IEEE802.22 standard.

This module is written in VHDL, capable of being used on any FPGA/ASIC architecture.

Performance

The following is the resource utilisation summary on a Kintex-7 410T part for data input bit width of 16, FFT size 128, power spectrum bit width of 18 and HMM window length of 5.

Slices	Block RAMs	Flip Flops
41763	15	41215