DVB-GSE Ethernet Tunnel IP Cores

DVB-GSE encapsulator and de-encapsulator IP cores with AXI4-Stream interconnect to/from (RG)MII interfaces.

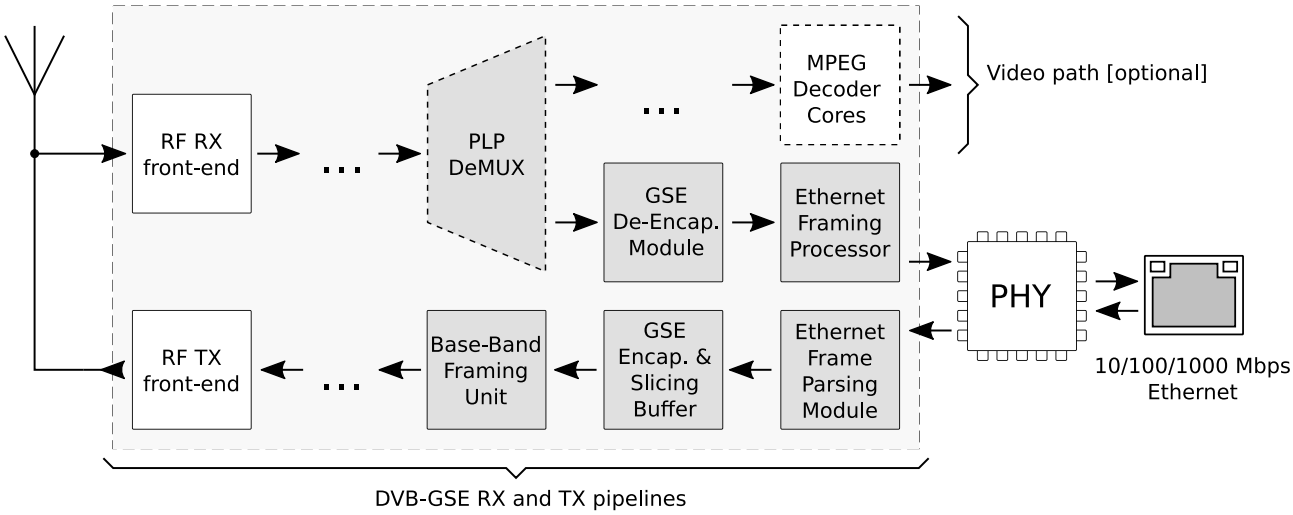

Figure 1: Block diagram for an example system containing an IP Core Worx DVB-GSE Ethernet Tunnel IP Cores

Overview:

High-throughput, low-latency Ethernet frame parsers & generators, and DVB-GSE encapsulator & de-encapsulator IP cores, for building datalink systems that transport Ethernet frames using DVB-GSE. The IP Core Worx DVB-GSE IP cores have been optimised for high performance, and also for DVB-S2/-T2/-C2 implementations that have strict resource/area constraints; for example, FPGA-based systems.

Pairing the IP Core Worx DVB-GSE Ethernet tunnel encapsulator core with its corresponding de-encapsulator core minimises the footprint & complexity of a bidirectional DVB-GSE system. (De-)Encapsulating of just layer 2 (Ethernet) traffic shifts the tasks of routing & QoS to external cores or devices (at each end of the Ethernet tunnel), increasing system flexibility and reducing FPGA resource requirements.

Features:

- GSE encapsulation of Ethernet frames (via the DVB-GSE *Bridged Frame Mandatory Extension Header*)
- Designed for high throughput and low latency
- Configurable MTU's, SRAM/buffer sizes, and packing & fragmentation modes
- Supports GSE packet header types for no labels, 6 byte labels, label reuse, and label-based filtering
- Low (logic and SRAM) resource usage
- Support for both 16200b and 64800b BBFRAME's, and all DATA FIELD sizes
- AXI4-Stream Interconnect (to/from PHY's and FEC units)
- Wishbone (SPEC B4) interface for control and packet/device statistics
- CRC-8 for BBFRAME's, and CRC-32 for reassembled PDU's and Ethernet frames
- Robust exception handling and with rapid recovery from exceptions (due to overflows & invalid input data)
- Can be configured for single- or dual- clock operation (if clock-domain crossing is required)
- FPGA-proven with Xilinx and Microsemi devices

Performance and Area:

The following table shows the resource utilisation for various IP Core Worx DVB-GSE cores, when using Xilinx Vivado for synthesis, and targeting Xilinx ZYNQ devices. The designs satisfy the timing constraints at more than 160 MHz (ZYNC devices) – exceeding GbE performance with FPGA-based designs.

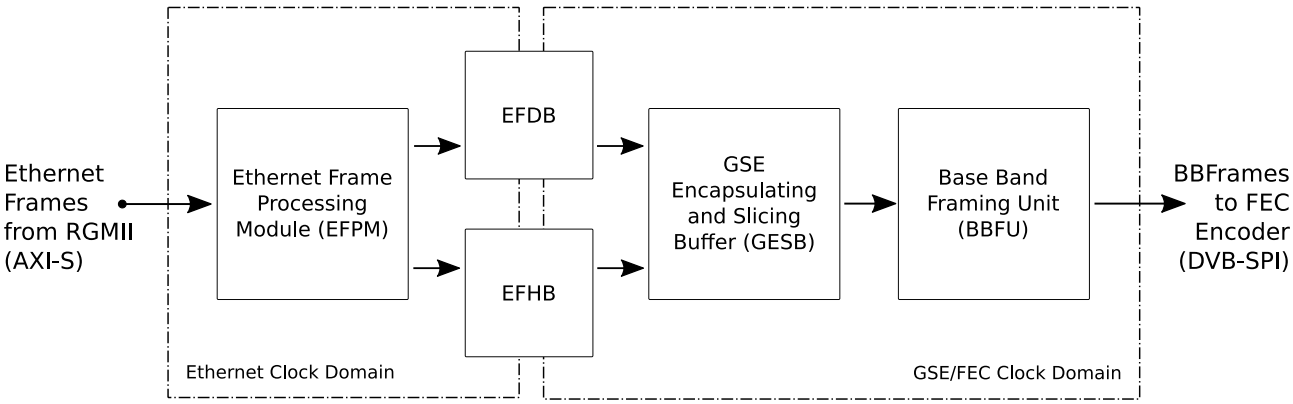

Figure 2: Block diagram for the system components of the IP Core Worx DVB-GSE Ethernet Tunnel, encapsulator datapath.

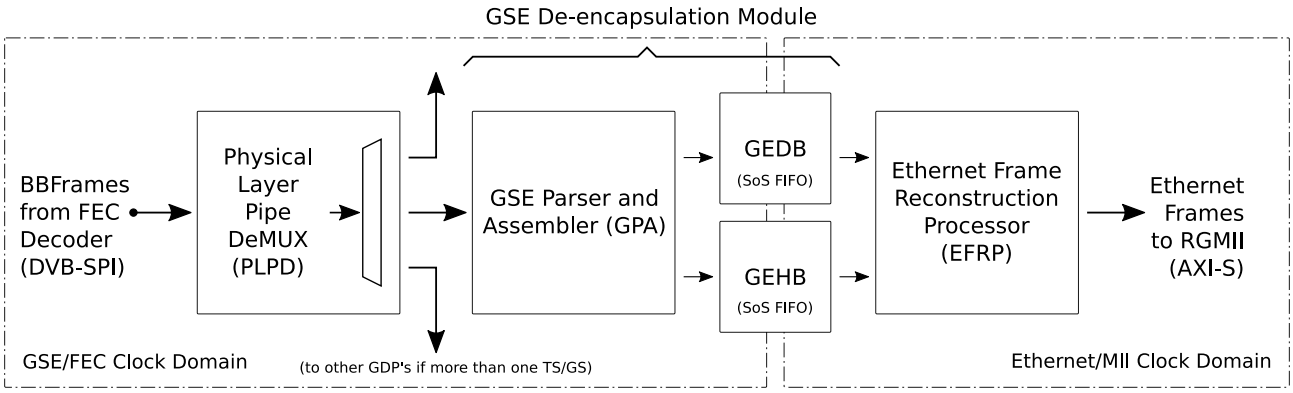

Figure 3: Block diagram for the system components of the IP Core Worx DVB-GSE Ethernet Tunnel, de-encapsulator datapath.

Resource	IP_TO_GSE	GSE_TO_IP	ETH_TO_GSE	GSE_TO_ETH
LUT6	720	303	1086	638
DFF	411	228	655	455
RAMB36	0.5	0.5	2	1.5
DSP	0	0	0	0
BUFG	1	1	1	1

Deliverables:

- Netlist or synthesisable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- User guides and documentation for integration & configuration
- Top-level entities for CCM-only, Ethernet-tunneling systems to aid with evaluation and rapid-prototyping