

# DVB-GSE IPv4/IPv6 De-encapsulator

DVB-GSE de-encapsulator IP cores for IPv4/IPv6 network-layer traffic, and utilising a DVB-SPI-like interconnect for received BBFRAME's, and AXI4-Stream interconnect for PDU output.

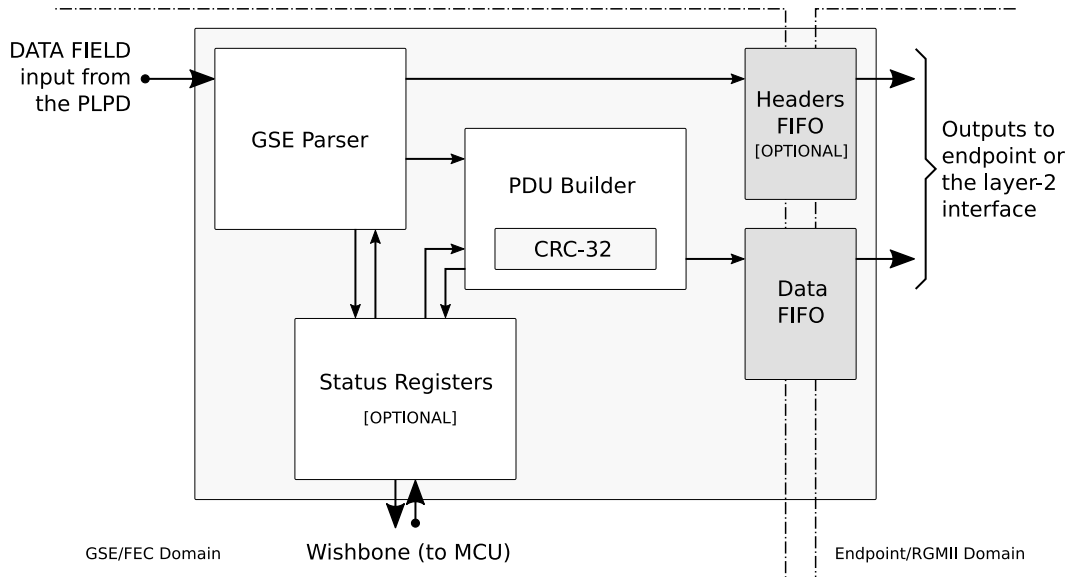


Figure 1: Block diagram showing the functional subunits of the IP Core Worx GSE De-encapsulator Module (GDM).

## Overview:

High-throughput, low-latency de-encapsulator IP cores for building DVB-GSE systems. The IP Core Worx DVB-GSE IP cores have been optimised for high performance, and also for DVB-S2/-T2/-C2 implementations that have strict resource/area constraints; for example, FPGA-based systems.

## Features:

- GSE de-encapsulation and PDU re-assembly for IPv4/IPv6 packets
- Designed for high throughput and low latency
- Supports GSE packet header types for no labels, 6 byte labels, label reuse, and label-based filtering
- Parameterisable MTU's and SRAM/buffer sizes
- Low (logic and SRAM) resource usage
- Support for both 16200b and 64800b BBFRAME's, and all DATA FIELD sizes
- AXI4-Stream (8-bit) Interconnect
- Wishbone (SPEC B4) interface for control and packet/device statistics
- Includes BBFRAME parser, stream de-MUX, and de-scrambling cores
- Robust exception handling and with rapid recovery from exceptions (due to overflows & invalid input data)
- FPGA-proven with Xilinx and Microsemi devices

## Performance and Area:

The following table shows the resource utilisation for various IP Core Worx DVB-GSE cores, when using Xilinx Vivado for synthesis, and targeting Xilinx ZYNQ devices. The designs satisfy the timing constraints at more than 160 MHz (ZYNC devices) – exceeding GbE performance with FPGA-based designs.

Resource	IP_TO_GSE	GSE_TO_IP	ETH_TO_GSE	GSE_TO_ETH
LUT6	720	303	1086	638
DFF	411	228	655	455
RAMB36	0.5	0.5	2	1.5

Resource	IP_TO_GSE	GSE_TO_IP	ETH_TO_GSE	GSE_TO_ETH
DSP	0	0	0	0
BUFG	1	1	1	1

## Deliverables:

- Netlist or synthesisable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- User guides and documentation for integration & configuration
- Top-level entity for a CCM-only system, to aid with evaluation and rapid-prototyping

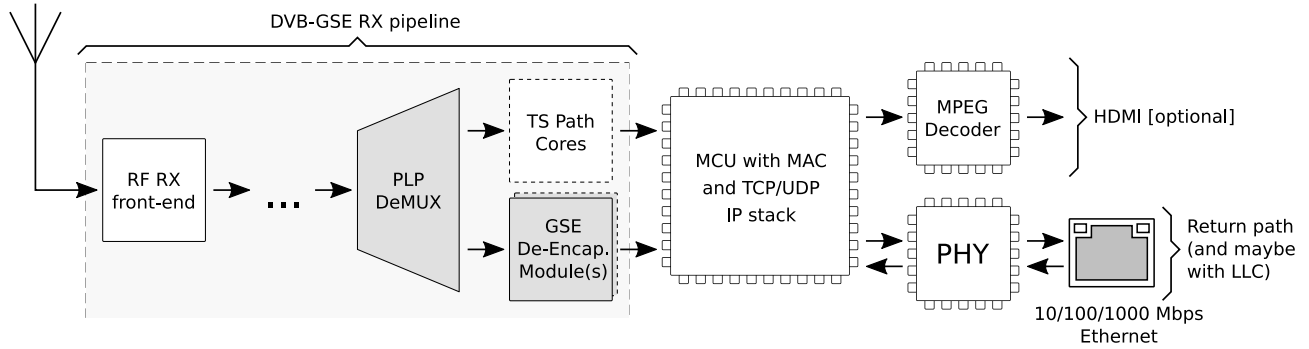


Figure 2: Block diagram for an example system containing an IP Core Worx DVB-GSE De-encapsulator IP Core.