Very Small Form-Factor Reciprocal Core

Clock
nReset
Input Width
Fraction Input Width
Input Data
Input Valid

Reciprocal Block

Output Data
Output Valid

Features

- Fast, power efficient, incredibly small form-factor reciprocal function.
- Parameterisable input widths
- Parameterisable fractional width input.
- Very close reciprocal approximate output.
- Area efficient design.
- Can be used in any hardware implementations where typically division may be avoided.
- Fully synchronous design using only one clock.
- No multipliers are used/required in the design.
- Form factor only dependent on input bit width. Area grows at a rate less than linear with input bit width.
- Silicon verified in multiple devices.

Deliverables

- Netlist or synthesizable RTL source code in VHDL.
- Comprehensive verification test bench and vectors in VHDL.
- Integration documentation and user guide.

Overview

This is a configurable reciprocal DSP core for signal processing application on programmable logic devices.

The core operates on streamed data which is reciprocated (inverse value calculated) via a non-traditional, intelligent, innovative design.

After an initial output delay equal to the bit width of the input plus 4 clock cycles, the output is also streamed out at a rate of one result per clock cycle.

This DSP engine is written in VHDL, capable of being used on any FPGA/ASIC architecture.

Performance

The following results compare the true floating-point reciprocal function (solid line) to the accuracy of the Reciprocal Core (dashed line) output for two different length input values. Note that these widths are parameterisable inputs.
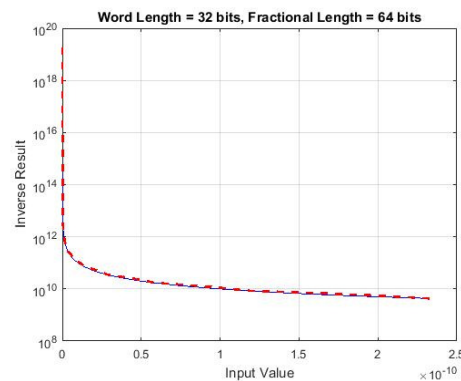
The following is the resource utilisation[1] for a Xilinx Virtex6 FPGA.

Input Width	Slices Used	Flip-Flops Used	Maximum Frequency
18 bit	267	576	346MHz
32 bit	397	551	389MHz

Note 1: Resource utilisation as reported by Xilinx ISE synthesiser. Utilisation may vary depending on application. Core clock rate depends on application.