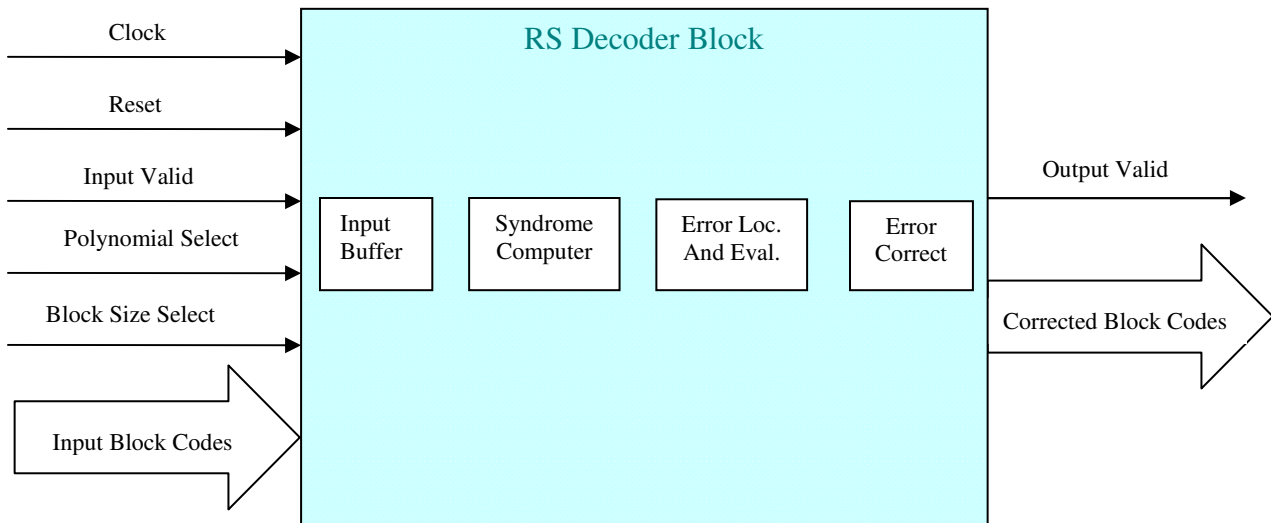# Reed-Solomon Decoder Core

Features
- Parameterisable primitive polynomial.
- Parameterisable symbol size (code block length)
- Parameterisable number of correctable errors
- Parameterisable input buffer size
- Decodes shortened and punctured codes
- Fully synchronous using single clock
- User friendly interface.
- Area efficient design
- Silicon verified in multiple devices
- Optimized for WMAN (802.16), DVB and other OFDM standards

Deliverables
- Netlist or synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- Integration documentation and user guide

Overview
Reed-Solomon (RS) decoder is ideal for correcting errors that occur in clusters.

Clustered bit errors are usual when there is frequency selective fading or multipath fading.

RS coding is a block coding technique. These codes are generally designated as (N,K,T) block codes. 'K' is the number of information symbols per block, 'N' is the number of symbols per block and T is the number of correctable errors.

This decoder is capable of decoding shortened and punctured coded. This can be controlled in real time allowing block by block code rate changes.

The RS Decoder is optimized for WiMAX. This core is written in VHDL, capable of being used on any FPGA/ASIC architecture.

Performance[1]
The following is the resource utilisation summary on a Spartan-3E part for the WiMAX RS code (N=255,K=239,T=8) over $GF(2^8)$ and generator polynomial $X^8+X^4+X^3+X^2+1$.

Slices	Block RAMs	Flip Flops
2410	3	3100

Note 1: Resource utilisation as reported by Xilinx ISE synthesiser. Utilisation may vary depending on application. Block RAM usage depends on input buffer size. Maximum core clock rate depends on application.