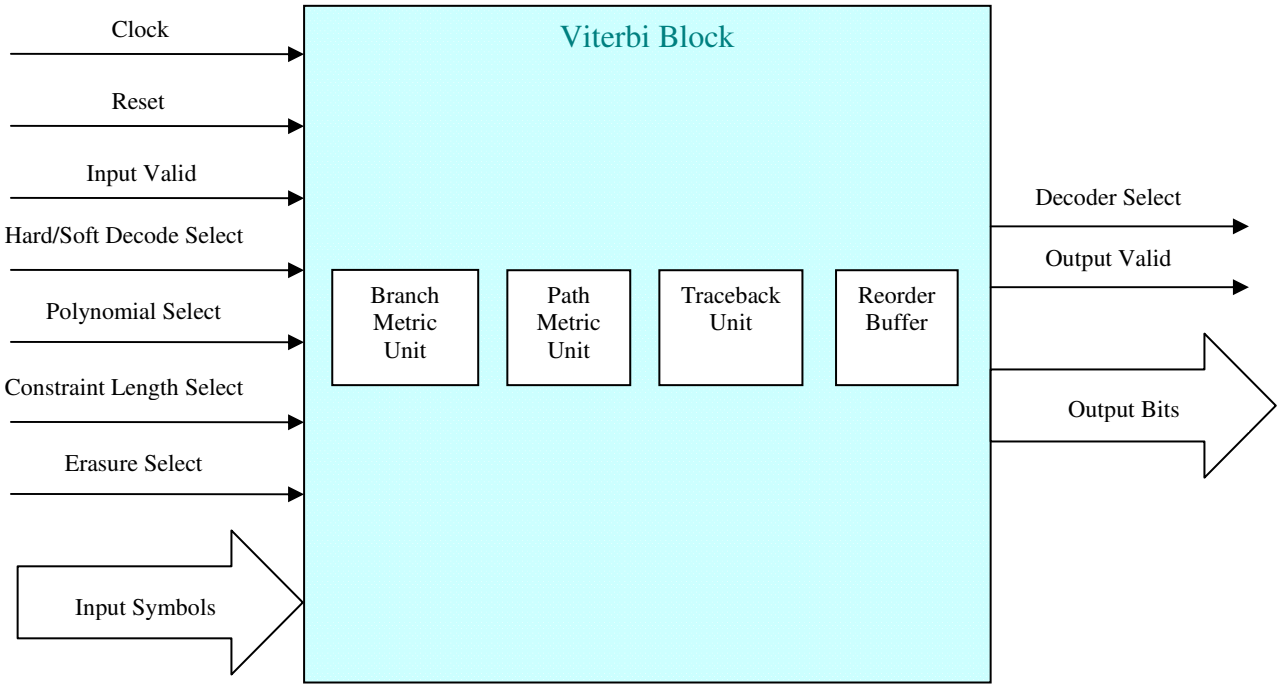
Viterbi Decoder Core



Features

- Hard or soft decoder with configurable soft bit widths
- Parameterisable generator polynomials
- Parameterisable code Constraint length
- Parameterisable trace-back length
- Support erasures (code puncturing)
- Fully synchronous design using only one clock
- 1 decoded bit per clock cycle throughput
- Automatic internal metric rescaling
- Low latency
- Optimized design allowing high-speed operation
- User friendly control interface
- Silicon verified in multiple devices
- Optimized for WLAN (802.11a/g, 802.16), DVB and other OFDM standards

Deliverables

- Netlist or synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- Integration documentation and user guide

Overview

Viterbi decoders are commonly used to decode convolutional codes in communications systems. This Viterbi Decoder is a fully parallel implementation which gives fast data throughput. The decoder is targeted for WiMax and Wireless LAN applications.

Input symbol metric pairs are decoded into output data bits by the maximum likelihood Viterbi processor core. Decoder supports both hard and soft inputs.

This decoder supports configurable traceback buffer size allowing performance to be fine tuned for different applications.

Codes with symbol erasures (punctured code) can be decoded by this decoder.

Processor core is optimized for decoding the 133,171 encoder used in 802.11a/g and 802.16 applications.

This decoder is written in VHDL, capable of being used on any FPGA/ASIC architecture.

Performance[1]

The following is the resource utilisation summary on a Spartan-3E part for the WiMAX ½ rate, constraint length 7, generator polynomial (171,133), Traceback length = 96 hard decision decoder.

Slices	Block RAMs	Flip Flops
1690	0	1160

The following is the resource utilisation summary on a Spartan-3E part for the WiMAX ½ rate, constraint length 7, generator polynomial (171,133), Traceback length = 96 soft decision decoder (3bit soft inputs).

Slices	Block RAMs	Flip Flops
2790	1	1900

Note 1: Resource utilisation as reported by Xilinx ISE synthesiser. Utilisation may vary depending on application. Block RAM usage depends on input buffer size and traceback buffer size. Maximum core clock rate depends on application.