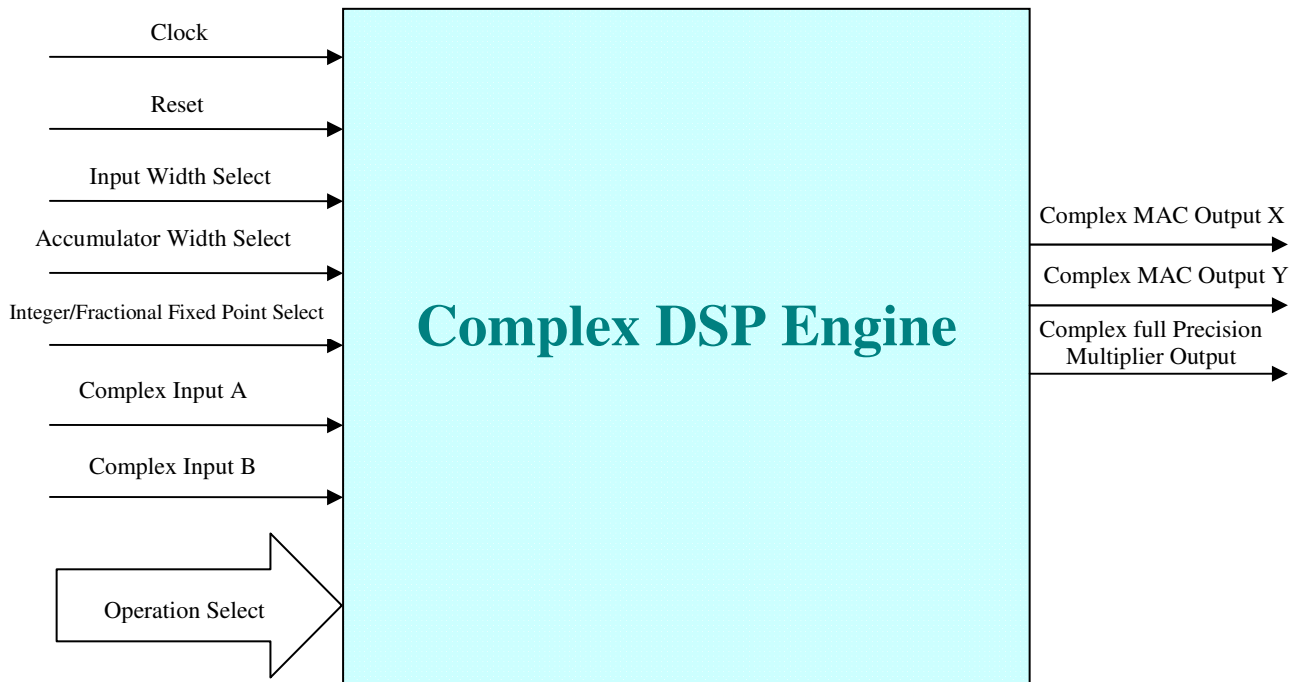


# Complex DSP Engine Core



## Features

- Consists of Conjugation unit, Complex Multiplier, Pre-adder and two Complex Accumulators (X and Y).
- Parameterizable input widths
- Parameterizable accumulator widths
- Full precision multiplier output available
- Integer and fractional fixed point arithmetic capability
- Supports operations such as Multiply, Multiply and Accumulate (Add/Subtract), Load Accumulator with external accumulator inputs, Multiply and Add/Subtract to external accumulator input and Multiply and Add/Subtract to external pre-add inputs.
- Supports common configurations such as MAC for Filters, FFT Butterfly, Correlation/Matched Filter and Sliding Window Correlator and many more.
- Fully synchronous design using only one clock
- User friendly control interface
- Silicon verified in multiple devices

## Deliverables

- Netlist or synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- Integration documentation and user guide

## Overview

This is a configurable complex DSP core for signal processing application on programmable logic devices. The core can be configured to perform some of the commonly used DSP functions such as digital filters, correlators and FFTs. The cores control signals allow the DSP function to be changed in real time hence allowing re-use of chip resources.

The core consists of a conjugation unit, a complex multiplier, a complex pre-adder and two configurable width complex accumulators (X and Y).

This DSP engine is written in VHDL, capable of being used on any FPGA/ASIC architecture.

# Performance<sup>1</sup>

The following is resource utilisation for a Xilinx Spartan3E part.

Multiplier Size	Accumulator Size	Slices Used	Flip-Flops Used	Multipliers Used (18X18)
18X18	44bits	780	800	4
32X32	72bits	2000	2600	16

Note 1: Resource utilisation as reported by Xilinx ISE synthesiser. Utilisation may vary depending on application. Core clock rate depends on application.

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