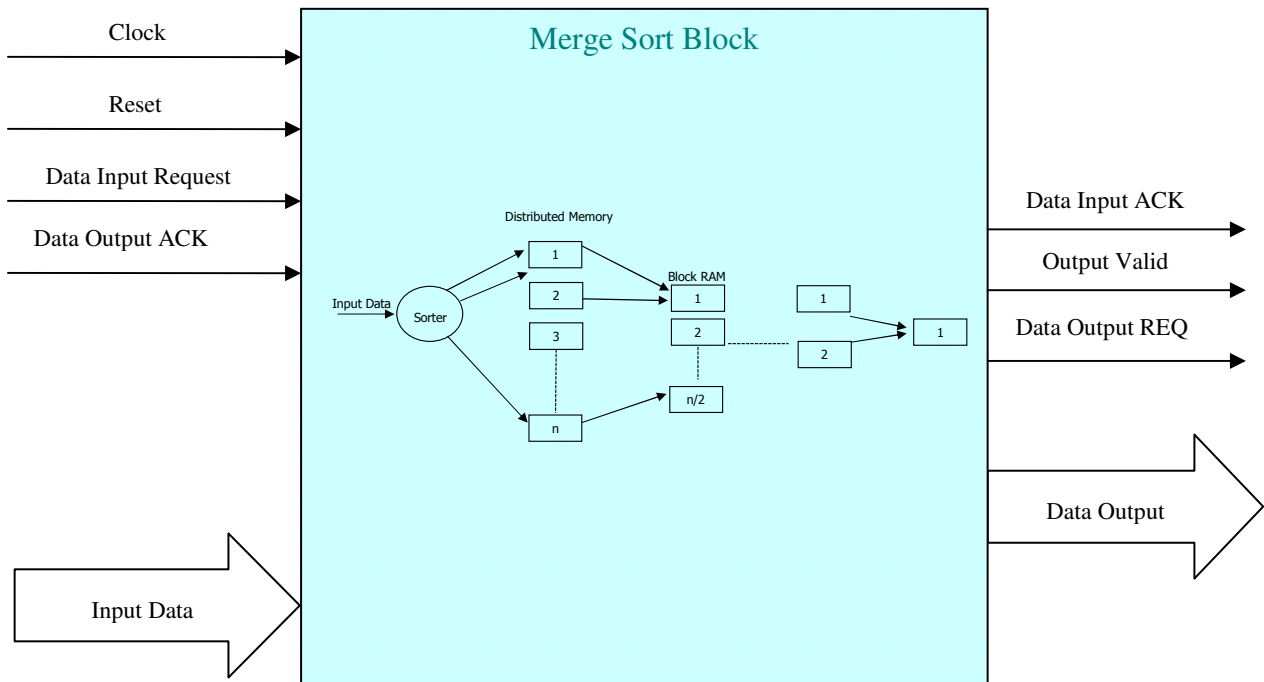


# Merge Sort Core



## Features

- Optimized design allows customers to target cost efficient FPGAs.
- Can be tailored to customer needs
- Fully synchronous design using only one clock
- Area/Power efficient architecture

## Deliverables

- Netlist or synthesizable RTL source code in VHDL
- Comprehensive verification test bench and vectors in VHDL
- Integration documentation and user guide

## Overview

This Merge Sort module is written in VHDL, capable of being used on any FPGA/ASIC architecture.

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